ABSTRACT OF THE DISCLOSURE

A nonvolatile semiconductor memory device having a small layout area includes a memory cell array in which a plurality of memory cells are arranged in a row direction and a column direction. The memory cell array includes: source line diffusion layers each of which is formed by connecting part of the memory cells in the row direction; bitline diffusion layers, isolation regions each of which divides one of the bitline diffusion layers, and word gate common connection sections. Each of the memory cells includes a word gate and a select gate. Each of the bitline diffusion layers is disposed between two of the word gates which are adjacent to each other in the column direction. Each of the word gate common connection sections connects the two adjacent word gates above the isolation regions.